EZReport Knowledge Extraction

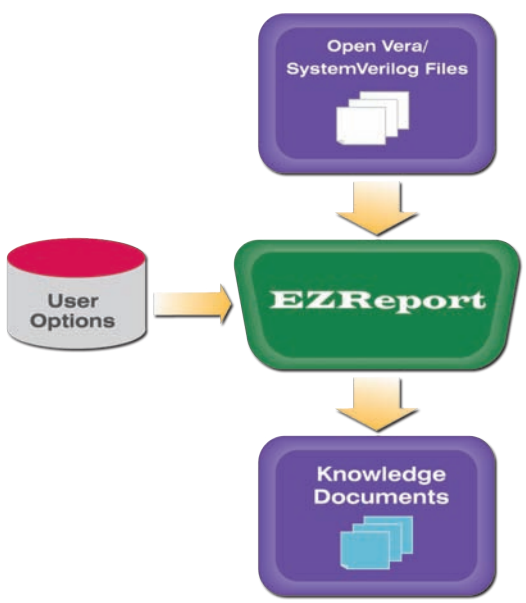
EZVerify : Verification Productivity with [EZReport] [EZCheck]

Verification Reuse can be a Reality

Verification reuse is a widely acknowledged solution for dealing with the exponential increase in verification time. The popularity of Hardware Verification Languages (HVL) for implementing test plans is the catalyst needed for making verification reuse a reality. The most important information needed in making reuse decisions in an HVL-based verification flow is a complete understanding of the component, module or object hierarchy at hand. However, very few easy-to-use tools exist that enable engineers to extract verification knowledge from modules.

EZReport is a tool designed to promote reuse within verification teams by providing comprehensive documentation that summarizes the verification aspects of any given HVL input.

Use Model



Benefits

- Provide instant reuse platform
- Create shareable, web-ready documents
- Consolidate and enable superior IP creation process
- Extract verification knowledge automatically
- View intuitive class hierarchy snapshot
- Summarize synchronization mechanisms

Features

- Full language support for OpenVera™ and SystemVerilog®
- Elegant integration with Doxygen
- HTML output with customizable style sheets
- Fits into existing flow
- High-performance - runs very fast
- Platforms - Solaris and Linux

Customizability

- **Input:** Create custom links in the table of contents, customize header files, author information and other specifics
- **Output:** Disable undesired sections from HTML output

VeriEZ Solutions, Inc. is a privately held company that develops and markets solutions that **enable efficient chip verification**. It is the developer of EZVerify and EZTranslate Tool Suites. EZVerify is the industry's first HVL productivity tool suite. EZTranslate is an OpenVera™-to-SystemVerilog® migration tool suite. **More information at www.veriez.com**

EZReport

Make No Changes in Your Existing Flow

EZReport is designed to work with an existing HVL-based verification flow. There is no need to change the way HVL modules are written. EZReport extracts knowledge and attaches documentation by following simple, but reasonable heuristics.

Information presented by EZReport includes:

- Top-level view
- Global variables and subroutines
- Object hierarchy
- Class data, including constraints and coverage models
- Class method hierarchy
- Connections between interfaces, ports and binds
- Property and sequence data (SystemVerilog only)
- Thread-specific information

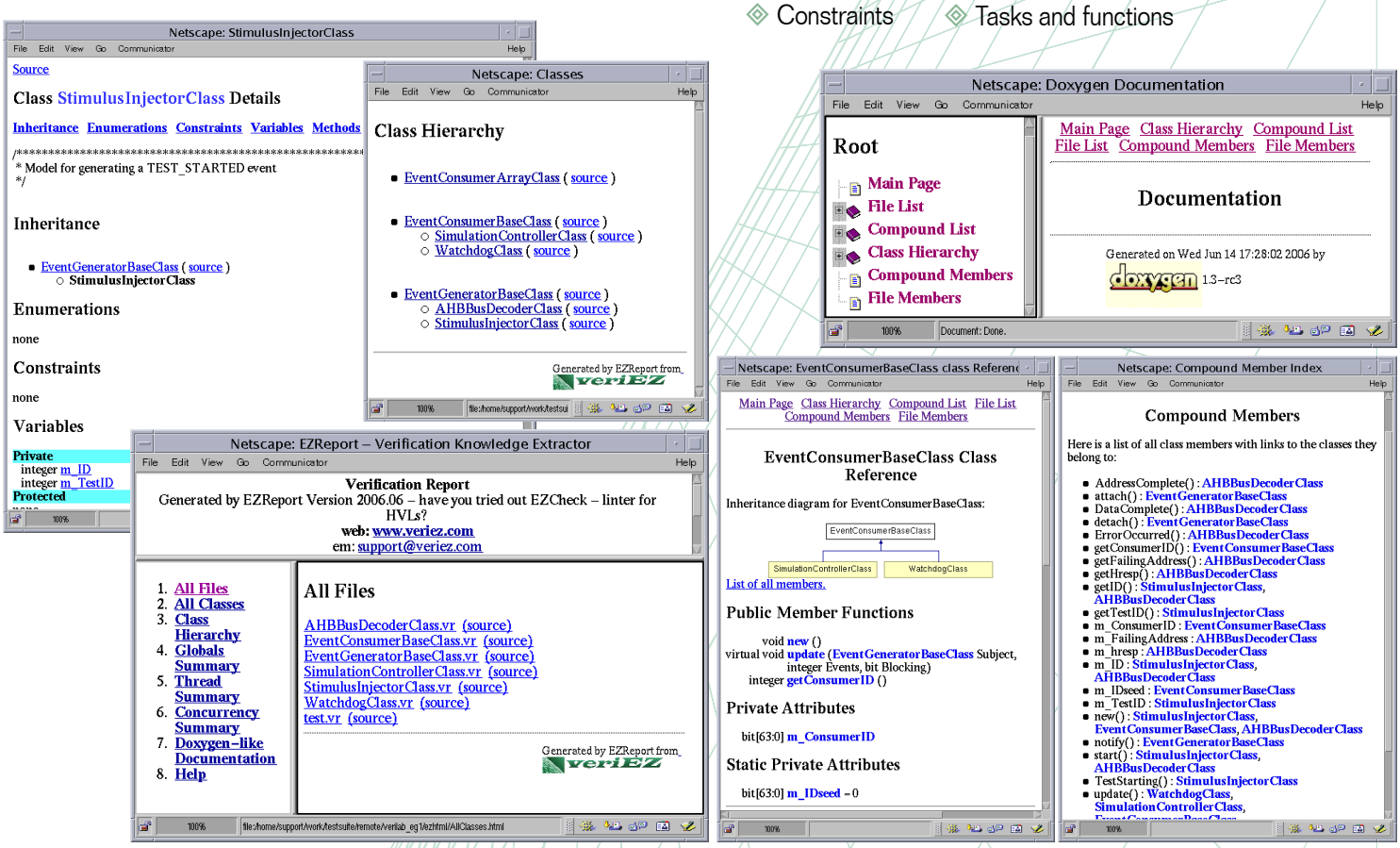
EZOxygen – Interface to Doxygen

Doxygen is a popular public-domain documentation system for common software programming languages such as C++, C and Java®. It is licensed under the GNU General Public License. Doxygen has the capability to automatically extract code structure and object information from program source files, including dependency graphs, inheritance diagrams and collaboration diagrams.

EZOxygen provides Doxygen capabilities for HVL input. EZOxygen's operation is tightly integrated with EZReport so that the user can quickly experience Doxygen-created documentation without requiring prior knowledge of the Doxygen usage model.

EZOxygen provides support for several HVL constructs, including:

- Classes
- Coverage Models
- Constraints
- Tasks and functions



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