Success Story: Cortina Systems

VeriEZ's EZVerify streamlines verification process at Cortina

Cortina Systems, Inc. is a technology and market leader enabling global communications. With R&D offices in USA, Canada and India, Cortina continues to execute on its complex design and verification flow.

The importance of efficient design and verification is well understood by Cortina's management. Cortina has consistently met customer requirements by bringing complex products to market in record time.

Verification productivity is key to delivering large-scale verification projects that are the norm at Cortina. In order to verify its products, it has put together a comprehensive methodology that leverages constraint-based randomization and object-oriented programming principles. Cortina continues to streamline its verification flow by incorporating the latest tools and technologies. EZCheck, VeriEZ's verification productivity solution, has been integrated into Cortina's verification flow to enable its engineers to develop robust and reusable verification plans.

The EZVerify Advantage

EZCheck Static Analysis
EZReport Knowledge Extraction

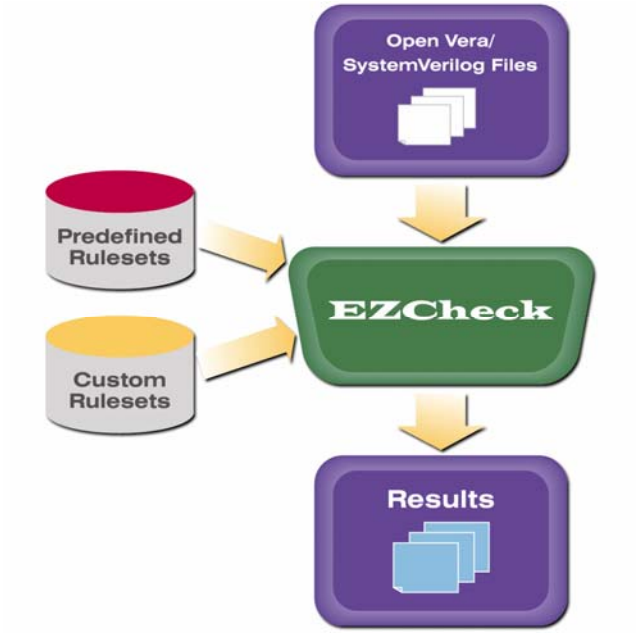
The challenge of verification is further intensified by the requirement to integrate a geographically dispersed engineering team with varying levels of experience. Cortina's verification team was able to leverage EZCheck in many ways. According to Andrew Peebles, Director of Engineering at Cortina Systems, "integration was fairly easy." Next, EZCheck was helpful in allowing the verification engineers to lint OpenVera™ code before it was passed to downstream simulators. Peebles and his team also defined extensions to existing rules such that the violations reported by EZCheck were consistent with the coding style prevalent at Cortina. VeriEZ's R&D team also added new functionality in EZCheck to generate constraint information.

As for EZReport's output, Peebles was very concise. "Pretty darn nice," he commented. In minutes, EZReport was able to extract and display concurrency information, class hierarchy, constraint data and other key verification information.

"If you take Verilog linting seriously, and have complex Vera testbenches, you'll love this tool. "

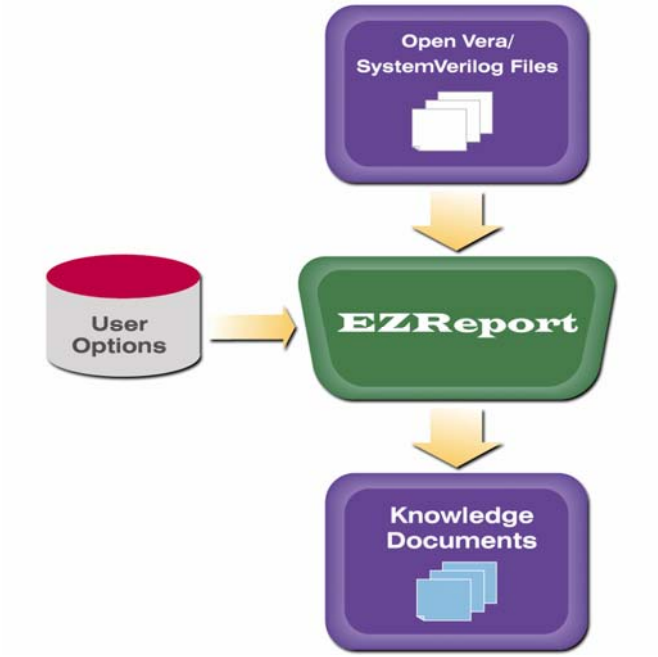
Andrew Peebles, Director of Engineering, Cortina Systems, Inc.

EZCheck Use Model



EZCheck enables users to exploit the power of static analysis for efficient design and verification by providing 325+ predefined rules and several “rulesets” that target error-free code development, best practices for functional coverage model design, object-oriented programming methodology, assertion-based verification and SystemVerilog® Migration.

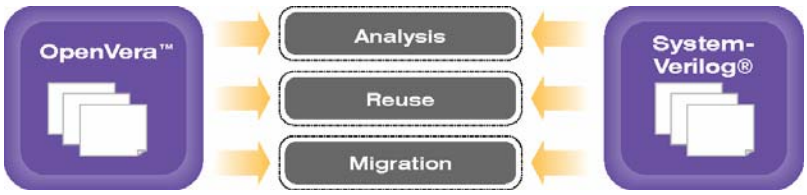
EZReport Use Model



EZReport is a tool designed to promote reuse within verification teams by providing comprehensive documentation that summarizes the verification aspects of any given HVL input. Information presented by EZReport includes global data, object hierarchy, class data (including constraints and coverage models), class method hierarchy and connection information.

Company Overview

VeriEZ was founded to address the need for tools that enable efficient verification. Every VeriEZ tool suite fits easily in existing end-user verification flow and provides immediate benefit to the customer. VeriEZ’s products combine new verification technologies with existing and evolving verification flows. Products include EZVerify, the industry’s first Hardware Verification Language productivity tool suite and EZTranslate, an OpenVera™-to-SystemVerilog® migration tool suite.



VeriEZ Solutions, Inc. is a privately held company that develops and markets solutions that enable efficient chip verification. It is the developer of EZVerify and EZTranslate Tool Suites. EZVerify is the industry’s first HVL productivity tool suite. EZTranslate is an OpenVera™-to-SystemVerilog® migration tool suite.

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