EZTranslate

The Industry's First Comprehensive Vera-to-SystemVerilog Migration Tool Suite

Over the past decade, Vera® has become a popular language to implement verification plans. Several companies building cutting-edge electronic products have used Vera successfully in their verification flow. SystemVerilog, the next generation of Verilog®, which includes verification-ready constructs is being viewed by users and vendors alike as a viable verification language. SystemVerilog-based verification teams can be vendor-independent, and realize cost-savings by utilizing the simulator's testbench capabilities.

EZTranslate provides a clear solution to companies seeking a Vera-to-SystemVerilog migration path. It can also be used to enforce a SystemVerilog-compatible Vera development policy for ongoing projects and to migrate existing Vera code to SystemVerilog.

Benefits

- Enforce SystemVerilog-compatible Vera development policy
- Reuse existing Vera modules in a SystemVerilog-based verification environment

Features

- Full language support for Vera
- User-extensible portability ruleset can be updated as the standard evolves
- Platforms: Solaris and Linux

About VeriEZ Solutions

VeriEZ Solutions, Inc. is a privately held company that develops and markets solutions that enable **efficient chip verification**. It is the developer of EZVerify and EZTranslate Tool Suites.

EZVerify is the industry's first OpenVera®/Vera® productivity Tool Suite. It includes a configurable static lint checker (EZCheck) and a verification knowledge extractor (EZReport). EZTranslate is a Vera-to-SystemVerilog® migration Tool Suite.

VeriEZ's tools detect errors and enable verification reuse. More information is available on the company website, www.veriez.com.

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OPENVERA Catalyst

SystemVerilog

EZTranslate

Vera-to-SystemVerilog Migration Tool Suite

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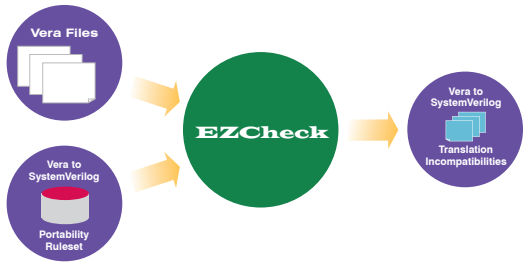
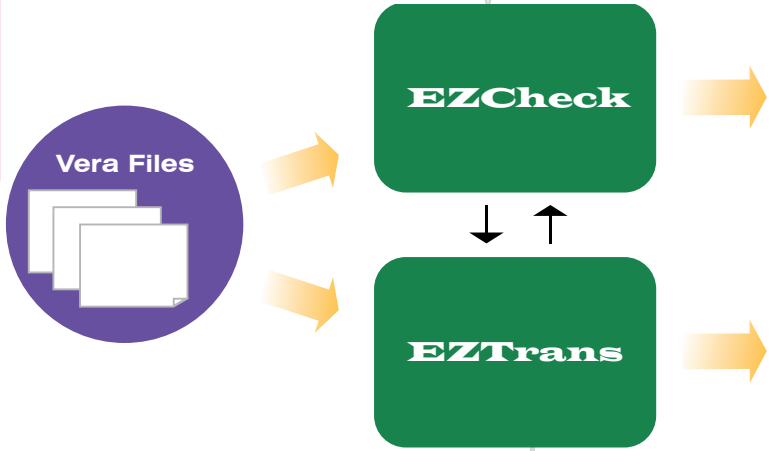
Vera-to-SystemVerilog Portability Ruleset

This user-customizable ruleset provides input to the EZCheck rule checker about constructs that will not be portable to the SystemVerilog environment. Examples of some of the checks included:

- Illegal identifiers
- Incompatible constructs (e.g. shadow variables)
- System Tasks and Functions with no SystemVerilog equivalent
- Incompatible operators (e.g. ><)
- Concurrency parameters (multiple buckets in semaphores)



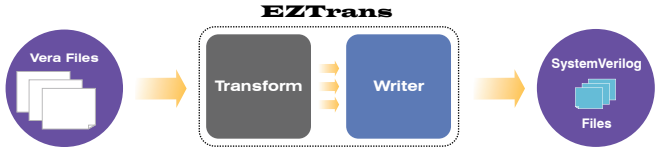


While translation may be the final objective, it is important to be able to determine and improve the"SystemVerilog-readiness" of input Vera code. EZTranslate provides this unique capability by detecting the incompatibilities and presenting them to the user in an HTML report. This feature can be used with ongoing projects as well as with legacy modules.

Translation Incompatibilities

SystemVerilog Files

The EZTrans writer creates SystemVerilog code. This can be used with any SystemVerilog-compatible simulator. Component boundaries, include files, and hierarchy are duplicated in the SystemVerilog output. Markers are provided in the source to locate constructs that could not be translated.



Transformations

Transformations change code "in memory" to create functionally equivalent and legal SystemVerilog code. Some of the transformations performed by EZTrans:

- Changing names of incompatible identifiers
- Transforming Sync calls with 'ORDER' to multiple sync calls
- Mapping system tasks and functions to equivalent calls
- Updating code that uses shadow variables to equivalent code without shadow variables

EZTranslate consists of two components:

1. EZCheck – a rule checker for detecting Vera constructs that will not port to SystemVerilog

2. EZTrans – a translator that transforms Vera to equivalent SystemVerilog source

EZCheck fulfills two key requirements:

1. It advises the user of "translation-readiness" before the actual translation. A translation and migration suite is incomplete without such a utility.

2. Tools and simulators that support SystemVerilog are not yet available for commercial use. EZCheck can be used to guide ongoing Vera development so that it may be translated without problems in the future.